

CLAIMS

What is claimed is:

- 005220-1952920
- 1 1. A system comprising:
- 2 a memory, wherein the memory includes a plurality of logical
- 3 memory devices; and
- 4 a network switch coupled to the memory, wherein the switch is
- 5 adaptable to write a first portion of received packet data to a first of the
- 6 plurality of logical memory devices and to write a second portion of the
- 7 packet data to a second of the plurality of logical memory devices.
- 1 2. The system of claim 1 wherein the network switch is further adaptable to
- 2 write a third portion of received packet data to a third of the plurality of logical
- 3 memory devices.
- 1 3. The system of claim 1 wherein the network switch comprises a memory
- 2 controller.
- 1 4. The system of claim 3 wherein the memory controller comprises:
- 2 a first memory controller component coupled to the first logical
- 3 memory device; and
- 4 a second memory controller component coupled to the second
- 5 logical memory device.

005564-022600

1 5. The system of claim 4 wherein the first memory controller component and
2 the second memory controller component access the corresponding logical
3 memory devices via a shared address line.

1 6. The system of claim 2 wherein the first, second and third logical memory
2 devices comprise synchronous dynamic random access memories (SDRAMs).

1 7. The system of claim 2 wherein the first logical memory devices comprises
2 a synchronous static random access memories (SSRAMs) and the second and
3 third logical memory devices comprise synchronous dynamic random access
4 memories (SDRAMs).

1 8. The system of claim 3 wherein the memory controller maintains a record
2 of the last of the plurality of logical memory devices that was written to.

1 9. The system of claim 3 wherein the network switch further comprises:
2 a receiver coupled to the memory controller;
3 a transmitter coupled to the memory controller;
4 address resolution logic coupled to the memory controller; and
5 packet queuing control coupled to the memory controller, the
6 receiver, the transmitter and the address resolution logic.

1 10. The system of claim 3 wherein the network switch further comprises a
2 media access controller (MAC) coupled to the receiver, wherein the MAC
3 receives packet data via a plurality of ports coupled to the receiver.

1 11. A network switch comprising:
2 a first media access controller (MAC) coupled to a plurality of
3 ports;
4 a receiver coupled to the first MAC; and
5 a memory controller coupled to the receiver, wherein the memory
6 controller is adaptable to write a first portion of a first data packet
7 received from a first of the plurality of ports to a first logical memory
8 device and write a second portion of the first data packet received from
9 the first port to a second logical memory device.

1 12. The system of claim 11 wherein the memory controller is further
2 adaptable to write a third portion of the first data packet received from the first
3 port to a third logical memory device.

1 13. The system of claim 11 wherein the memory controller is adaptable to
2 write a first portion of a second data packet received from the first port to a third
3 logical memory device and write a second portion of the second data packet
4 received from the first port to a fourth logical memory device.

1 14. The system of claim 11 wherein the memory controller is adaptable to
2 write a first portion of a first data packet received from a second of the plurality
3 of ports to the first logical memory device and write a second portion of the first
4 data packet received from the second port to a second logical memory device.

1 15. The system of claim 11 wherein the memory controller comprises:
2 a first memory controller component coupled to the first logical
3 memory device; and
4 a second memory controller component coupled to the second
5 logical memory device.

1 16. The system of claim 15 wherein the first memory controller component
2 and the second memory controller component access the corresponding logical
3 memory devices via a shared address line.

1 17. The system of claim 12 wherein the first, second and third logical memory
2 devices comprise synchronous dynamic random access memories (SDRAMs).

1 18. The system of claim 12 wherein the first logical memory devices
2 comprises a synchronous static random access memories (SSRAMs) and the
3 second and third logical memory devices comprise synchronous dynamic
4 random access memories (SDRAMs).

Sub A17

009220-1952500

1 19. A method comprising:
2 receiving a first data packet at a network switch;
3 writing a first portion of the first data packet to a first logical
4 memory device coupled to the network switch; and
5 writing a second portion of the first data packet to a second logical
6 memory device coupled to the network switch.

1 20. The method of claim 19 further comprising writing a third portion of the
2 first data packet to a third logical memory device coupled to the network switch.

1 21. The method of claim 19 further comprising:
2 receiving a second data packet at a network switch;
3 writing a first portion of the second data packet to the first logical
4 memory device; and
5 writing a second portion of the second data packet to the second
6 logical memory device.

1 22. The method of claim 19 further comprising determining at the network
2 switch the last logical memory device to which a portion of the first data packet
3 was written.

1 23. The method of claim 22 further comprising:

2 determining whether the size of a third portion of the first data
3 packet is less than a predetermined value; and
4 if so, writing the third portion of the second data packet to both
5 banks of a third logical memory device.

1 24. The method of claim 22 further comprising:

2 determining whether the size of a third portion of the first data
3 packet is less than a predetermined value; and
4 if not, writing a first sub-portion of the third portion of the first
5 data packet to a first bank of a third logical memory device and writing a
6 second sub-portion of the third portion of the first data packet to a second
7 bank of the third logical memory device.